PRELIMINARY

#295255

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# 8293
# GPIB TRANSCEIVER

- Nine Open-collector or Three-state Line Drivers
- 48 mA Sink Current Capability on Each Line Driver
- Nine Schmitt-type Line Receivers
- High Capacitance Load Drive Capability
- Single 5V Power Supply
- 28-Pin Package
- Low Power HMOS Design
- On-chip Decoder for Mode Configuration
- Power Up/Power Down Protection to Prevent Disrupting the IEEE Bus
- Connects with the 8291A and 8292 to Form an IEEE Standard 488 Interface Talker/Listener/Controller with no Additional Components
- Only Two 8293's Required per GPIB Interface
- On-Chip IEEE-488 Bus Terminations

The Intel® 8293 GPIB Transceiver is a high-current, non-inverting buffer chip designed to interface the 8291A GPIB Talker/Listener, or the 8291A/8292 GPIB Talker/Listener/Controller combination, to the IEEE Standard 488-1978 Instrumentation Interface Bus. Each GPIB interface would contain two 8293 Bus Transceivers. In addition, the 8293 can also be used as a general-purpose bus driver.

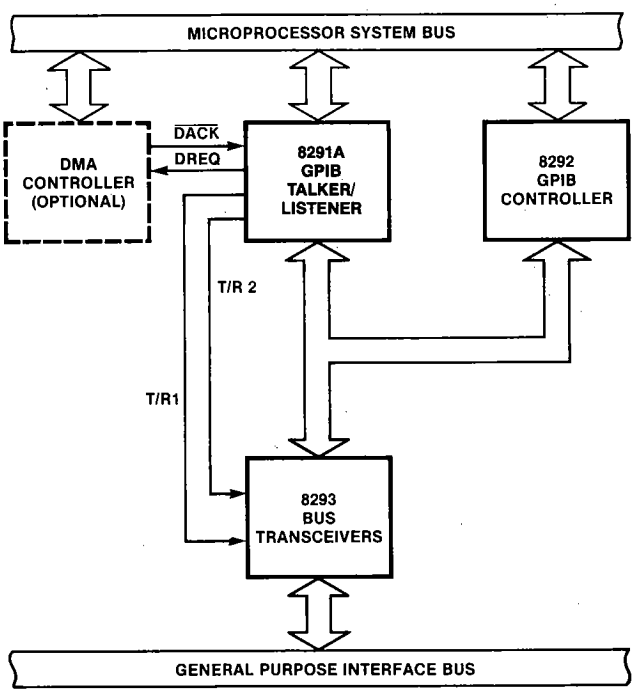



Figure 1. 8291A, 8292, 8293 Block Diagram

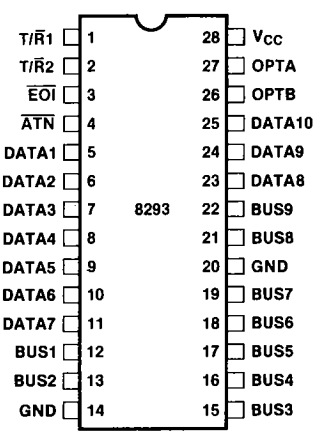



Figure 2. Pin Configuration

## Table 1. Pin Description

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| BUS1-BUS9 | 12, 13, 15–19, 21, 22 | I/O | **GPIB Lines, GPIB Side:** These are the IEEE-488 bus interface driver/receivers, or TTL-compatible inputs on the 8291A/8292 side, depending on the mode used. Their use is programmed by the two mode select pins, OPTA and OPTB. |
| DATA1-DATA10 | 5–11, 23–25 | I/O | **GPIB Lines, 8291A/92 Side:** These are the pins to be connected to the 8291A and 8292 to interface with the GPIB. Their use is programmed by the two mode select pins, OPTA and OPTB. All these pins are TTL compatible. |
| T/$\overline{R}$1 | 1 | I | **Transmit Receive 1:** This pin controls the direction for NDAC, NRFD, DAV, and DIO1-DIO8. Input is TTL compatible. |
| T/$\overline{R}$2 | 2 | I | **Transmit Receive 2:** This pin controls the direction for EOI. Input is TTL compatible. |
| $\overline{EOI}$ | 3 | I/O | **End Or Identify:** This pin indicates the end of a multiple byte transfer or, in conjunction with ATN, addresses the device during a polling sequence. It connects to the 8291A and is switched between transmit and receive by T/$\overline{R}$2. This pin is TTL compatible. |
| $\overline{ATN}$ | 4 | O | **Attention:** This pin is used by the 8291A to monitor the GPIB ATN control line. It specifies how data on the DIO lines is to be interpreted. This output is TTL compatible. |
| OPTA<br>OPTB | 27<br>26 | I<br>I | **Mode Select:** These two pins are to control the function of the 8293. A truth table of how they program the various modes is in Table 2. |
| $V_{CC}$ | 28 | P.S. | **Voltage:** Positive power supply (5V ± 10%). |
| GND | 14, 20 | P.S. | **Ground:** Circuit ground. |

## Table 2. 8293 Mode Selection Pin Mapping

| Pin Name | Pin No. | IEEE Implementation Name | | | |
|---|---|---|---|---|---|
| | | Mode 0 | Mode 1 | Mode 2 | Mode 3 |
| OPTA | 27 | 0 | 1 | 0 | 1 |
| OPTB | 26 | 0 | 0 | 1 | 1 |
| DATA1 | 5 | $\overline{IFC}$ | $\overline{DIO8}$ | $\overline{IFC}$ | $\overline{DIO8}$ |
| BUS1 | 12 | IFC* | DIO8* | IFC* | DIO8* |
| DATA2 | 6 | $\overline{REN}$ | $\overline{DIO7}$ | $\overline{REN}$ | $\overline{DIO7}$ |
| BUS2 | 13 | REN* | DIO7* | REN* | DIO7* |
| DATA3 | 7 | NC | $\overline{DIO6}$ | $\overline{EOI2}$ | $\overline{DIO6}$ |
| BUS3 | 15 | EOI* | DIO6* | EOI* | DIO6* |
| DATA4 | 8 | $\overline{SRQ}$ | $\overline{DIO5}$ | $\overline{SRQ}$ | $\overline{DIO5}$ |
| BUS4 | 16 | SRQ* | DIO5* | SRQ* | DIO5* |
| DATA5 | 9 | $\overline{NRFD}$ | $\overline{DIO4}$ | $\overline{NRFD}$ | $\overline{DIO4}$ |
| BUS5 | 17 | NRFD* | DIO4* | NRFD* | DIO4* |
| DATA6 | 10 | $\overline{NDAC}$ | $\overline{DIO3}$ | $\overline{NDAC}$ | $\overline{DIO3}$ |
| BUS6 | 18 | NDAC* | DIO3* | NDAC* | DIO3* |
| DATA7 | 11 | T/$\overline{R}$IO1 | NC | $\overline{ATNI}$ | $\overline{ATNO}$ |
| DATA8 | 23 | T/$\overline{R}$IO2 | $\overline{DIO2}$ | $\overline{ATNO}$ | $\overline{DIO2}$ |
| BUS7 | 19 | ATN* | DIO2* | ATN* | DIO2* |
| DATA9 | 24 | $\overline{GIO1}$ | $\overline{DAV}$ | $\overline{CIC}$ | $\overline{DAV}$ |
| BUS8 | 21 | GIO1* | DAV* | CLTH | DAV* |
| DATA10 | 25 | $\overline{GIO2}$ | $\overline{DIO1}$ | $\overline{IFCL}$ | $\overline{DIO1}$ |
| BUS9 | 22 | GIO2* | DIO1* | SYC | DIO1* |
| T/$\overline{R}$1 | 1 | T/$\overline{R}$1 | T/$\overline{R}$1 | T/$\overline{R}$1 | T/$\overline{R}$1 |
| T/$\overline{R}$2 | 2 | T/$\overline{R}$2 | NC | T/$\overline{R}$2 | $\overline{IFCL}$ |
| $\overline{EOI}$ | 3 | $\overline{EOI}$ | $\overline{EOI}$ | $\overline{EOI}$ | $\overline{EOI}$ |
| $\overline{ATN}$ | 4 | $\overline{ATN}$ | $\overline{ATN}$ | $\overline{ATN}$ | $\overline{ATN}$ |

***Note:** These pins are the IEEE-488 bus non-inverting driver/receivers. They include all the bus terminations required by the Standard and may be connected directly to the GPIB bus connector.

## GENERAL DESCRIPTION

The 8293 is a bidirectional transceiver. It was designed to interface the Intel 8291A GPIB Talker/Listener and the Intel® 8292 GPIB Controller to the IEEE Standard 488-1978 Instrumentation Bus (also referred to as the GPIB). The Intel GPIB Transceiver meets or exceeds all of the electrical specifications defined in the IEEE Standard 488-1978, Section 3.3–3.5, including the bus termination specifications.

The 8293 can be hardware programmed to one of four modes of operation. These modes allow the 8293 to be configured to support both a Talker/Listener/Controller environment and a Talker/Listener environment. In addition, the 8293 can be used as a general-purpose, three-state (push-pull) or open-collector bus transceiver with nine receiver/drivers. Two modes each are used to support a Talker/Listener (see Figure 3) and a Talker/Listener/Controller environment (see Figure 4). Mode 1 is used in general-purpose environments.

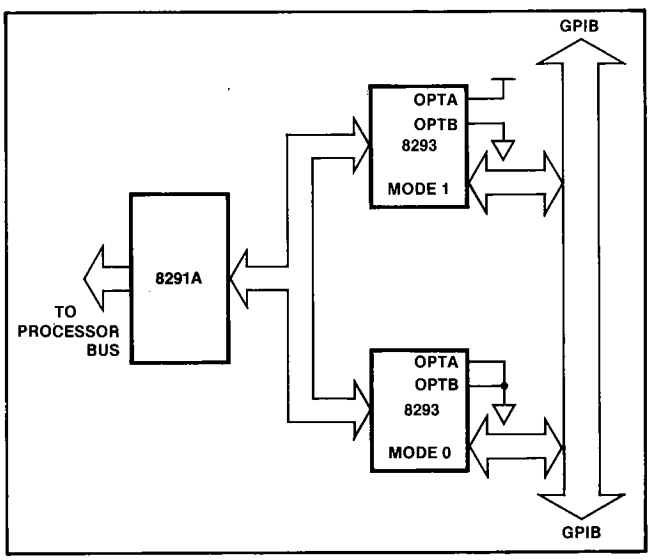



**Figure 3. Talker/Listener Configuration**

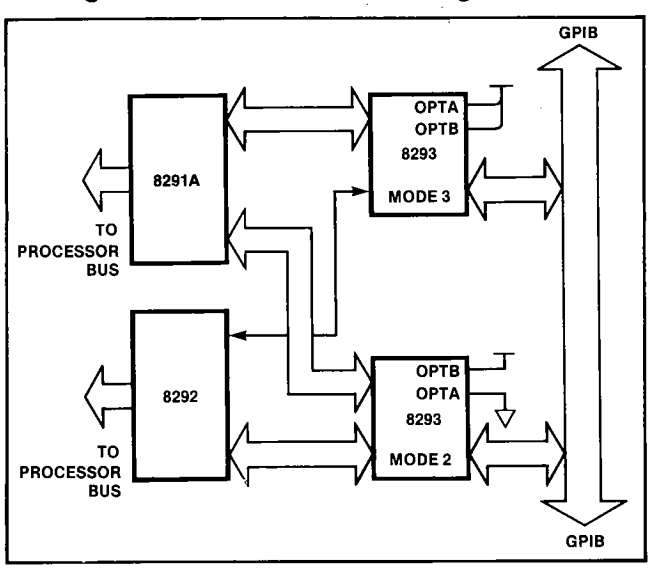



**Figure 4. Talker/Listener/Controller Configuration**

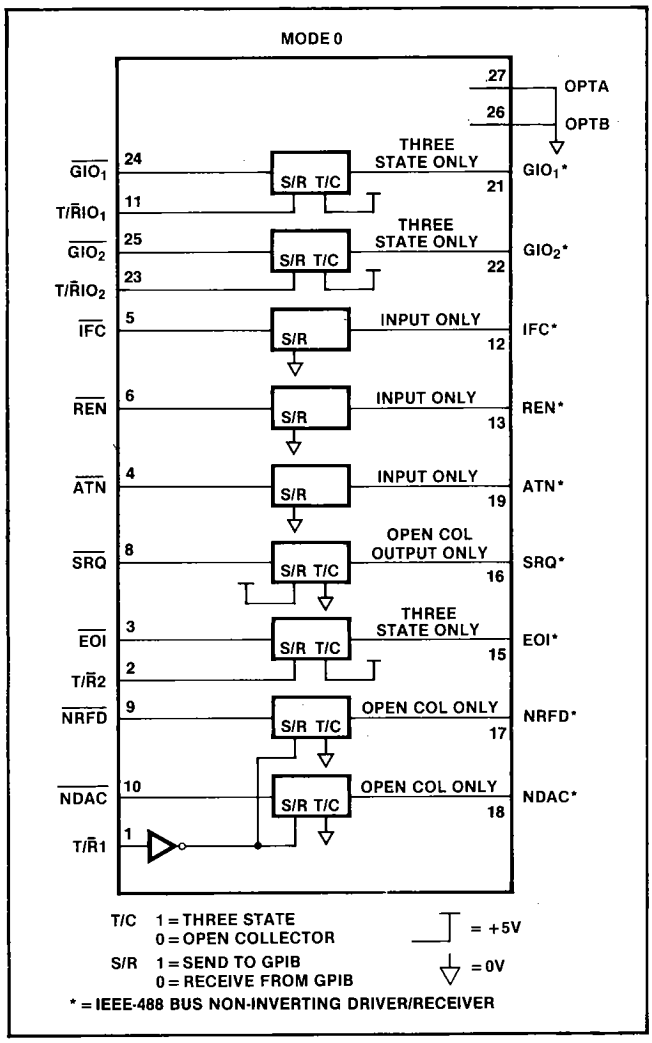



**Figure 5. Talker/Listener Control Configuration**

**Table 3. Mode 0 Pin Description**

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| T/$\overline{R}$1 | 1 | I | **Transmit Receive 1** Direction control for NDAC and NRFD. If T/R1 is high, then NDAC* and NRFD* are receiving. Input is TTL compatible. |
| $\overline{NDAC}$ | 10 | I/O | **Not Data Accepted:** Processor GPIB bus handshake control line; used to indicate the condition of acceptance of data by device(s). It is TTL compatible. |
| NDAC* | 18 | I/O | **Not Data Accepted:** IEEE GPIB bus handshake control line. When an input, it is a TTL compatible Schmitt-trigger. When an output, it is an open-collector driver with 48 mA sinking capability. |
| $\overline{NRFD}$ | 9 | I/O | **Not Ready For Data:** Processor GPIB handshake control line; used to indicate the condition of readiness of device(s) to accept data. This pin is TTL compatible. |

## Table 3. Mode 0 Pin Description (Continued)

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| NRFD* | 17 | I/O | **Not Ready For Data:** IEEE GPIB bus handshake control line. When an input, it is a TTL compatible Schmitt-trigger. When an output, it is an open-collector driver with a 48 mA current sinking capability. |
| T/$\overline{R}$2 | 2 | I | **Transmit Receive 2:** Direction control for EOI. If T/R2 is high, EOI* is sending. Input is TTL compatible. |
| $\overline{EOI}$ | 3 | I/O | **End Or Identify:** Processor GPIB bus control line; is used by a talker to indicate the end of a multiple byte transfer. This pin is TTL compatible. |
| EOI* | 15 | I/O | **End Or Identify:** IEEE GPIB bus control line; is used by a talker to indicate the end of a multiple byte transfer. This pin is a three-state (push-pull) driver capable of sinking 48 mA and a TTL compatible receiver with hysteresis. |
| $\overline{SRQ}$ | 8 | I | **Service Request:** Processor GPIB bus control line; used by a device to indicate the need for service and to request an interruption of the current sequence of events on the GPIB. It is a TTL compatible input. |
| SRQ* | 16 | O | **Service Request:** IEEE GPIB bus control line; it is an open collector driver capable of sinking 48 mA. |
| $\overline{REN}$ | 6 | O | **Remote Enable:** Processor GPIB bus control line; used by a controller (in conjunction with other messages) to select between two alternate sources of device programming data (remote or local control). This output is TTL compatible. |
| REN* | 13 | I | **Remote Enable:** IEEE GPIB bus control line. This input is a TTL compatible Schmitt-trigger. |
| $\overline{ATN}$ | 4 | O | **Attention:** Processor GPIB bus control line; used by the 8291 to determine how data on the DIO signal lines are to be interpreted. This is a TTL compatible output. |
| ATN* | 19 | I | **Attention:** IEEE GPIB bus control line; this input is a TTL compatible Schmitt-trigger. |
| $\overline{IFC}$ | 5 | O | **Interface Clear:** Processor GPIB bus control line; used by a controller to place the interface system into a known quiescent state. It is a TTL compatible output. |
| IFC* | 12 | I | **Interface Clear:** IEEE GPIB bus control line. This input is a TTL compatible Schmitt-trigger. |
| T/$\overline{R}$IO1<br>T/$\overline{R}$IO2 | 11<br>23 | I<br>I | **Transmit Receive General IO:** Direction control for the two spare transceivers. These pins are TTL compatible. |
| $\overline{GIO1}$<br>$\overline{GIO2}$ | 24<br>25 | I/O<br>I/O | **General IO:** This is the TTL side of the two spare transceivers. These pins are TTL compatible. |
| GIO1*<br>GIO2* | 21<br>22 | I/O<br>I/O | **General IO:** These are spare three-state (push-pull) drivers/Schmitt-trigger receivers. The drivers can sink 48 mA. |

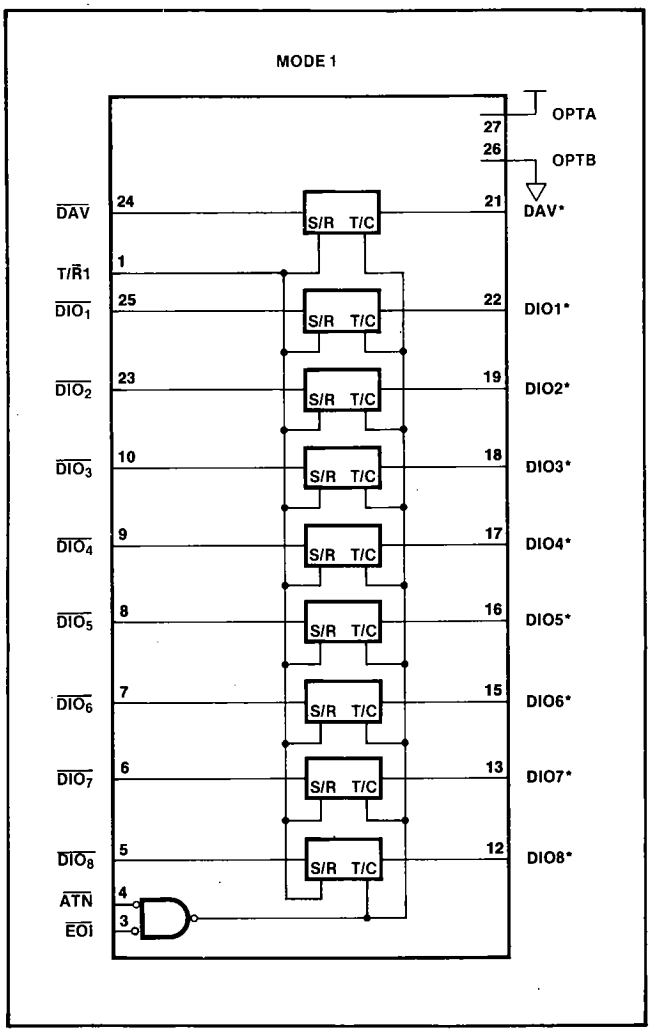



**Figure 6. Talker/Listener Data Configuration**

## Table 4. Mode 1 Pin Description

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| T/$\overline{R1}$ | 1 | I | **Transmit Receive 1:** Controls the direction for DAV and the DIO lines. If T/$\overline{R1}$ is high, then all these lines are sending information to the IEEE GPIB lines. This input is TTL compatible. |
| $\overline{EOI}$<br>$\overline{ATN}$ | 3<br>4 | I<br>I | **End Of Sequence And Attention:** Processor GPIB control lines. These two control signals are ANDed together to determine whether all the transceivers in the 8293 are three-state (push-pull) or open-collector. When both signals are low (true), then the controller is performing a parallel poll and the transceivers are all open-collector. These inputs are TTL compatible. |
| $\overline{DAV}$ | 24 | I/O | **Data Valid:** Processor GPIB bus handshake control line; used to indicate the condition (availability and validity) of information on the DIO lines. It is TTL compatible. |
| DAV* | 21 | I/O | **Data Valid:** IEEE GPIB bus handshake control line. When an input, it is a TTL compatible Schmitt-trigger. When DAV* is an output, it can sink 48 mA. |
| $\overline{DIO1}$-<br>$\overline{DIO8}$ | 25, 23,<br>10, 9,<br>8, 7,<br>6, 5 | I/O | **Data Input/Output:** Processor GPIB bus data lines; used to carry message and data bytes in a bit-parallel byte-serial form controlled by the three handshake signals. These lines are TTL compatible. |
| DIO1*-<br>DIO8* | 22, 19,<br>18, 17,<br>16, 15,<br>13, 12 | I/O | **Data Input/Output:** IEEE GPIB bus data lines. They are TTL compatible Schmitt-triggers when used for input and can sink 48 mA when used for output. See $\overline{ATN}$ and $\overline{EOI}$ description for output mode. |

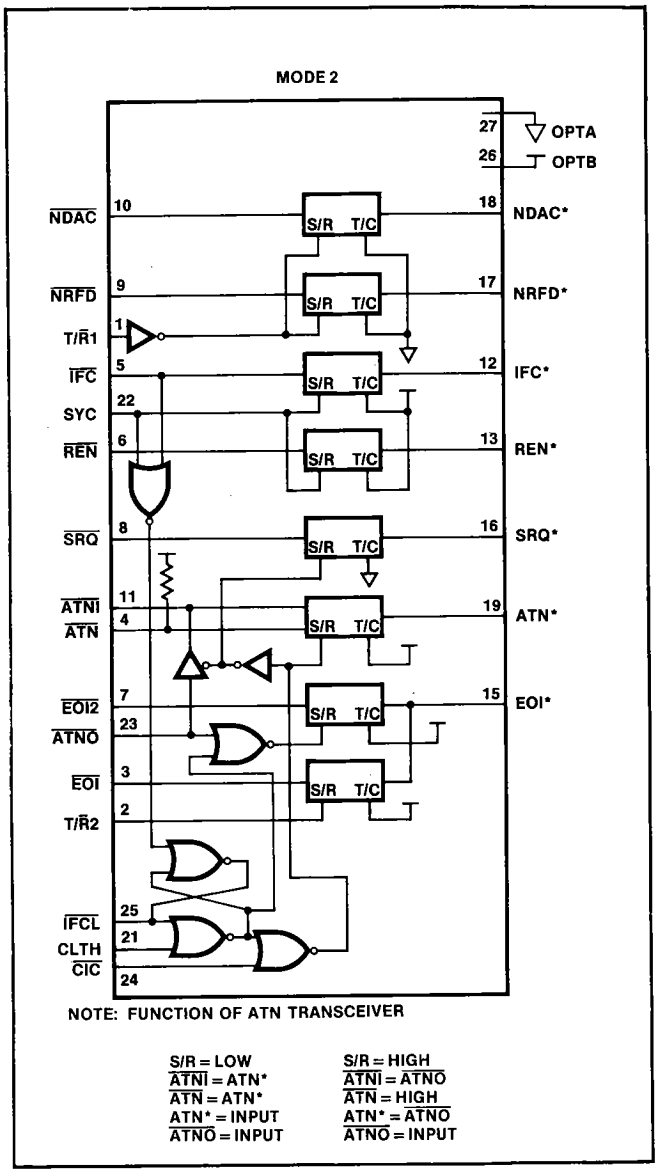



**Figure 7. Talker/Listener/Controller Control Configuration**

## Table 5. Mode 2 Pin Description

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| T/$\overline{R1}$ | 1 | I | **Transmit Receive 1:** Direction control for NDAC and NRFD. If T/$\overline{R1}$ is high, then NDAC and NRFD are receiving. Input is TTL compatible. |
| $\overline{NDAC}$ | 10 | I/O | **Not Data Accepted:** Processor GPIB bus handshake control line; used to indicate the condition of acceptance of data by device(s). This pin is TTL compatible. |
| NDAC* | 18 | I/O | **Not Data Accepted:** IEEE GPIB bus handshake control line. It is a TTL compatible Schmitt-trigger when used for input and an open-collector driver with a 48 mA current sink capability when used for output. |
| $\overline{NRFD}$ | 9 | I/O | **Not Ready For Data:** Processor GPIB bus handshake control line; used to indicate the condition of readiness of device(s) to accept data. This pin is TTL compatible. |
| NRFD* | 17 | I/O | **Not Ready For Data:** IEEE GPIB bus handshake control line. It is a TTL compatible Schmitt-trigger when used for input and an open-collector driver with a 48 mA current sink capability when used for output. |
| SYC[1] | 22 | I | **System Controller:** Used to monitor the system controller switch and control the direction for IFC and REN. This pin is a TTL compatible input. |
| $\overline{REN}$ | 6 | I/O | **Remote Enable:** Processor GPIB control line; used by the active controller (in conjunction with other messages) to select between two alternate sources of device programming data (remote or local control). This pin is TTL compatible. |
| REN* | 13 | I/O | **Remote Enable:** IEEE GPIB bus control line. When used as an input, this is a TTL compatible Schmitt-trigger. When an output, it is a three-state driver with a 48 mA current sinking capability. |
| $\overline{IFC}$ | 5 | I/O | **Interface Clear:** Processor GPIB bus control line; used by the active controller to place the interface system into a known quiescent state. This pin is TTL compatible. |
| IFC* | 12 | I/O | **Interface Clear:** IEEE GPIB control line. This is a TTL compatible Schmitt-trigger when used for input and a three-state driver capable of sinking 48 mA current when used for output. |
| $\overline{CIC}$ | 24 | I | **Controller In Charge:** Used to control the direction of the SRQ and to indicate that the 8292 is in charge of the bus. $\overline{CIC}$ is a TTL compatible input. |
| CLTH[1] | 21 | I | **Clear Latch:** Used to clear the IFC Received latch after it has been recognized by the 8292. Normally low (except after a hardware reset). It will be pulsed high when IFC Received is recognized by the 8292. This input is TTL compatible. |
| $\overline{IFCL}$ | 25 | O | **IFC Received Latch:** The 8292 monitors the IFC line when it is not the active controller through this pin. |
| $\overline{SRQ}$ | 8 | I/O | **Service Request:** Processor GPIB control line; indicates the need for attention and requests the active controller to interrupt the current sequence of events on the GPIB bus. This pin is TTL compatible. |
| SRQ* | 16 | I/O | **Service Request:** IEEE GPIB bus control line. When used as an input, this pin is a TTL compatible Schmitt-trigger. When used as an output, it is an open-collector driver with a 48 mA current sinking capability. |
| T/$\overline{R2}$ | 2 | I | **Transmit Receive 2:** Controls the direction for EOI. This input is TTL compatible. |
| $\overline{ATNO}$ | 23 | I | **Attention Out:** Processor GPIB bus control line; used by the 8292 for ATN control of the IEEE bus during "take control synchronously" operations. A low on this input causes ATN to be asserted if $\overline{CIC}$ indicates that this 8292 is in charge. $\overline{ATNO}$ is a TTL compatible input. |
| $\overline{ATNI}$ | 11 | O | **Attention In:** Processor GPIB bus control line; used by the 8292 to monitor the ATN line. This output is TTL compatible. |
| $\overline{ATN}$ | 4 | O | **Attention:** Processor GPIB bus control line; used by the 8292 to monitor the ATN line. This output is TTL compatible. |
| ATN* | 19 | I/O | **Attention:** IEEE GPIB bus control line; used by a controller to specify how data on the DIO signal lines are to be interpreted and which devices must respond to data. When used as an output, this pin is a three-state driver capable of sinking 48 mA current. As an input, it is a TTL compatible Schmitt-trigger. |
| $\overline{EOI2}$ | 7 | I/O | **End Or Identify 2:** Processor GPIB bus control line; used in conjunction with ATN by the active controller (the 8292) to execute a polling sequence. This pin is TTL compatible. |
| $\overline{EOI}$ | 3 | I/O | **End Or Identify:** Processor GPIB bus control line; used by a talker to indicate the end of a multiple byte transfer sequence. This pin is TTL compatible. |

**NOTES:**

1. $V_{IL3}$ is guaranteed at 1.1V on these inputs to accommodate the high current-sourcing capability of these pins during a low input in Mode 2.

**Table 5. Mode 2 Pin Description (Continued)**

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| EOI* | 15 | I/O | **End Or Identify:** IEEE GPIB bus control line; used by a talker to indicate the end of a multiple byte transfer sequence or, by a controller in conjunction with ATN, to execute a polling sequence. When an output, this pin can sink 48 mA current. When an input, it is a TTL compatible Schmitt-trigger. |

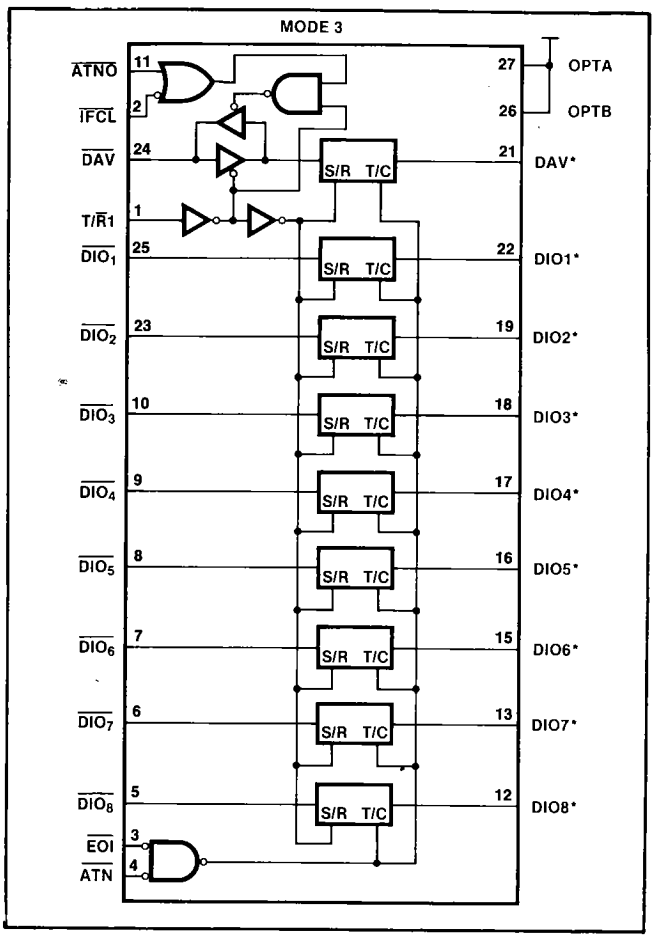



**Figure 8. Talker/Listener/Controller Data Configuration**

**Table 6. Mode 3 Pin Description**

| Symbol | Pin No. | Type | Name and Function |
|---|---|---|---|
| T/$\overline{R1}$ | 1 | I | **Transmit Receive 1:** Controls the direction for DAV and the DIO lines. If T/$\overline{R1}$ is high, then all these lines are sending information to the IEEE GPIB lines. This input is TTL compatible. |
| $\overline{EOI}$<br>$\overline{ATN}$ | 3<br>4 | I<br>I | **End Of Sequence and Attention:** Processor GPIB control lines. These two control lines are ANDed together to determine whether all the transceivers in the 8293 are push-pull or open-collector. When both signals are low (true), then the controller is performing a parallel poll and the transceivers are all open-collector. These inputs are TTL compatible. |
| $\overline{ATNO}$ | 11 | I | **Attention Out:** Processor GPIB control line; used by the 8292 during "take control synchronously" operations. This pin is TTL compatible. |
| $\overline{IFCL}$ | 2 | I | **Interface Clear Latched:** Used to make DAV received after the system controller asserts IFC. This input is TTL compatible. |
| $\overline{DAV}$ | 24 | I/O | **Data Valid:** Processor GPIB handshake control line; used to indicate the condition (availability and validity) of information on the DIO signals. This pin is TTL compatible. |
| DAV* | 21 | I/O | **Data Valid:** IEEE GPIB handshake control line. When an input, this pin is a TTL compatible Schmitt-trigger. When DAV* is an output, it can sink 48 mA. |
| $\overline{DIO1}$-<br>$\overline{DIO8}$ | 25, 23, 10, 9, 8, 7, 6, 5 | I/O | **Data Input/Output:** Processor GPIB bus data lines; used to carry message and data bytes in a bit-parallel byte-serial from controlled by the three handshake signals. These lines are TTL compatible. |
| DIO1*<br>DIO8* | 22, 19, 18, 17, 16, 15, 13, 12 | I/O | **Data Input/Output:** IEEE GPIB bus data lines. They are TTL compatible Schmitt-triggers when used for input and can sink 48 mA when used for output. |

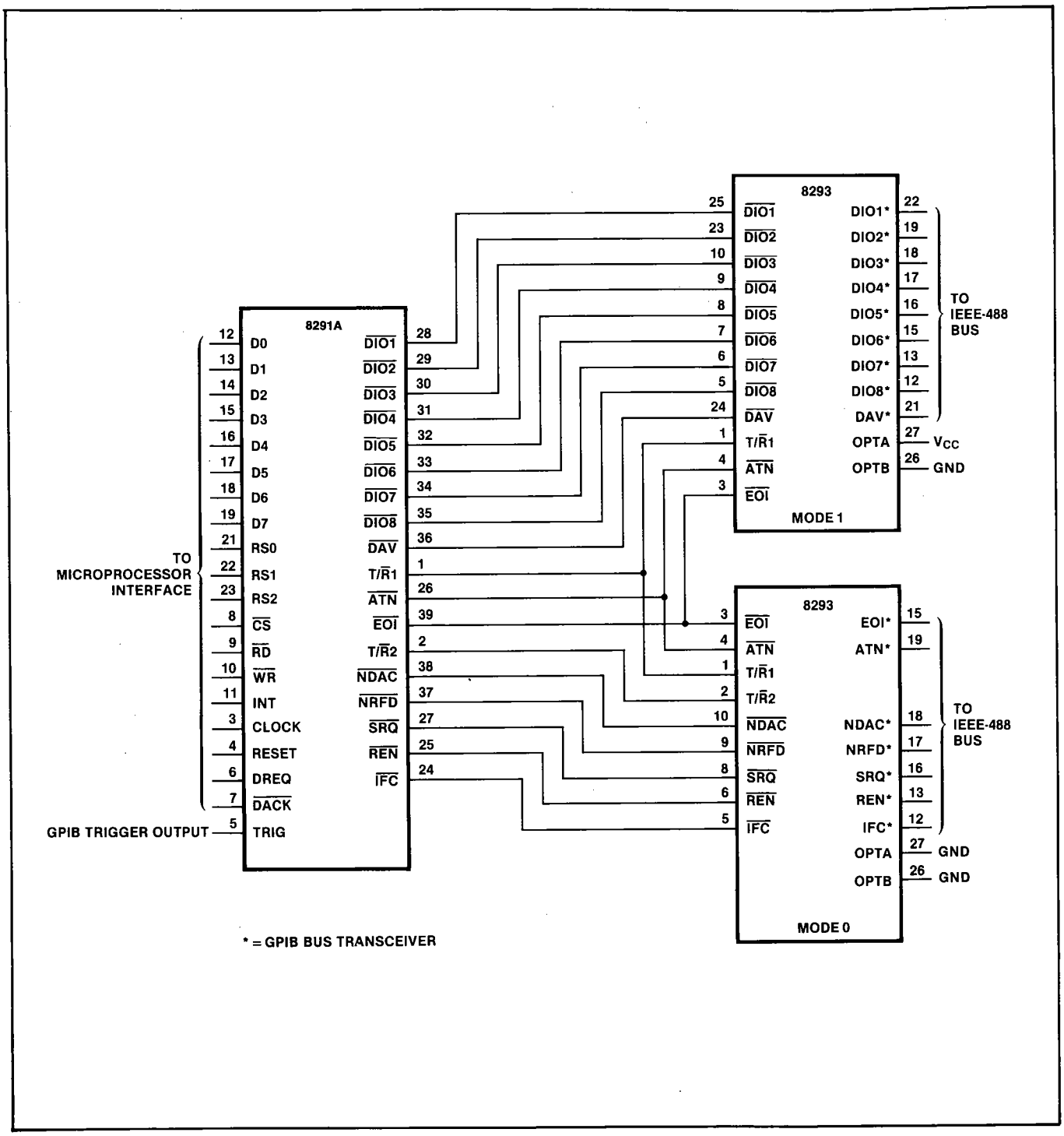



**Figure 9. 8291A and 8293 System Configuration**

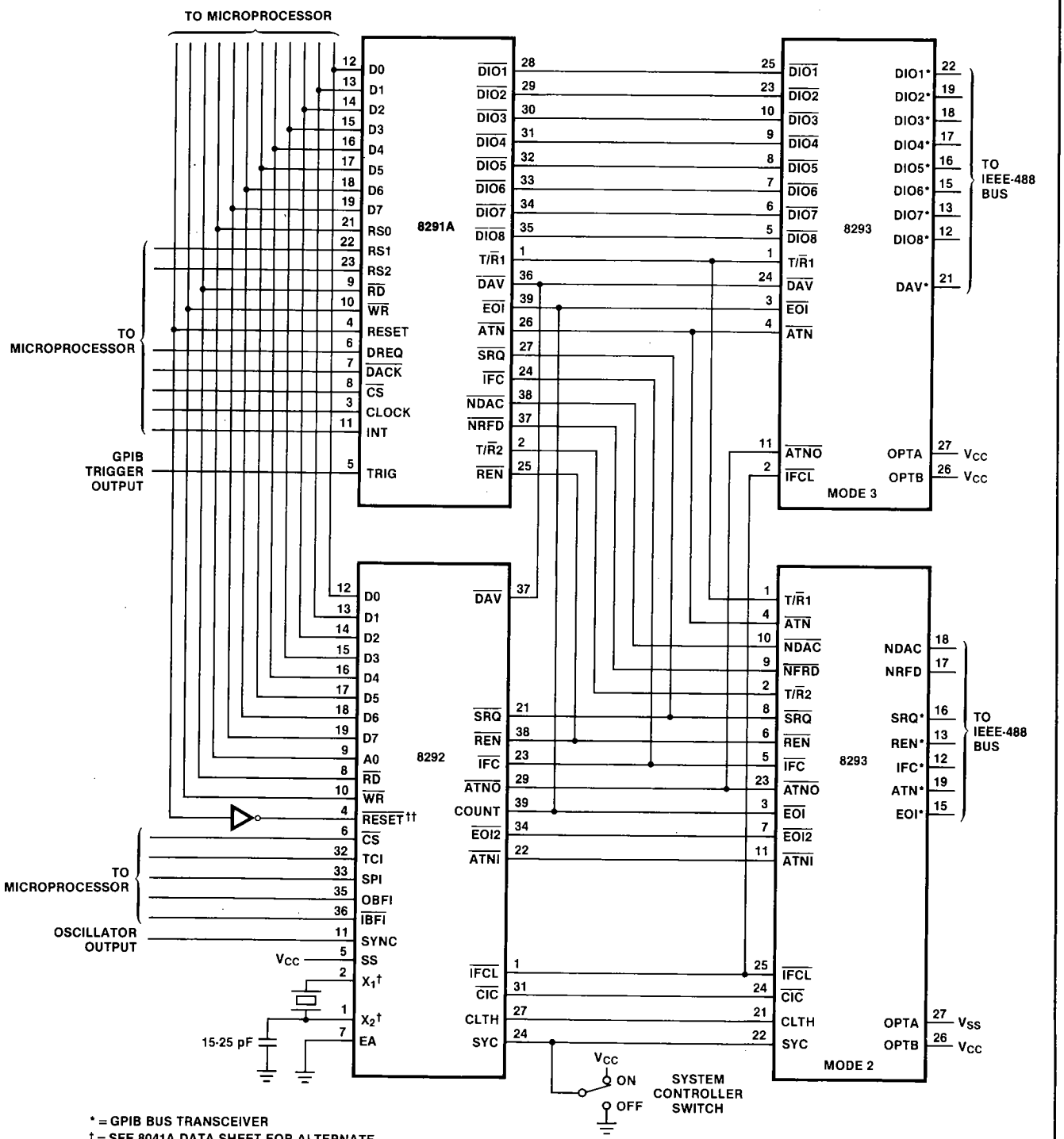



**Figure 10. 8291A, 8292, and 8293 System Configuration**

## ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on any Pin with
Respect to Ground . . . . . −1.0V to +7V
Power Dissipation . . . . . 1 Watt

*NOTICE:
*1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
*2. All devices are guaranteed to operate within the minimum and maximum parameter limits specified below. Typical parameters however are not tested and are not guaranteed. Established statistically, they indicate the performance level expected in a typical device at room temperature ($T_A$ = 25°C) and $V_{CC}$ = 5V.*

## D.C. CHARACTERISTICS ($T_A$ = 0°C to 70°C, $V_{CC}$ = 5.0V ±10%, GND = 0V)

| Symbol | Parameter | Limits | | | Units | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{IL1}$ | Input Low Voltage (GPIB Bus Pins) | | | 0.8 | V | |
| $V_{IL2}$ | Input Low Voltage (Option Pins) | −0.1 | | 0.1 | V | |
| $V_{IL3}$[1] | Input Low Voltage (All Others) | | | 0.8 | V | |
| $V_{IH1}$ | Input High Voltage (GPIB Bus Pins) | 2.0 | | $V_{CC}$ | V | |
| $V_{IH2}$ | Input High Voltage (Option Pins) | 4.5 | | $V_{CC}$ | V | |
| $V_{IH3}$ | Input High voltage (All Others) | 2.0 | | $V_{CC}$ | V | |
| $V_{IH4}$ | Receiver Input Hysteresis | 400 | | | mV | |
| $V_{OL1}$ | Output Low Voltage (GPIB Bus Pins) | | | 0.5 | V | $I_{OL}$ = 48 mA |
| $V_{OL2}$ | Output Low Voltage (All Others) | | | 0.5 | V | $I_{OL}$ = 16 mA |
| $V_{OH1}$ | Output High Voltage (GPIB Bus Pins) | 2.4 | | | V | $I_{OH}$ = −5.2 mA |
| $V_{OH2}$ | Output High Voltage (All Others) | 2.4 | | | V | $I_{OH}$ = −800 μA |
| $V_{IT}$ | Receiver Input Threshold High to Low | 0.8 | | | V | |
| | Receiver Input Threshold Low to High | | | 2.0 | | |
| $I_{LC}$ | Input Load Current (GPIB Pins) | See Bus Load Line Diagram | | | | $V_{CC}$ = 5.0V ± 5% |
| $I_{IL}$ | Input Leakage Current (All Others) | | | 10 | μA | 0.45 ≤ $V_{IN}$ ≤ $V_{CC}$ |
| $I_{PD}$ | Bus Power Down Leakage Current | | | 40 | μA | 0.45V ≤ $V_{BUS}$ ≤ 2.7V |
| $I_{CC}$ | Power Supply Current | | 110 | 175 | mA | |

**NOTES:**
1. $V_{IL3}$ = 1.1V max on pins 21 and 22 in Mode 2 for the 8293-10.

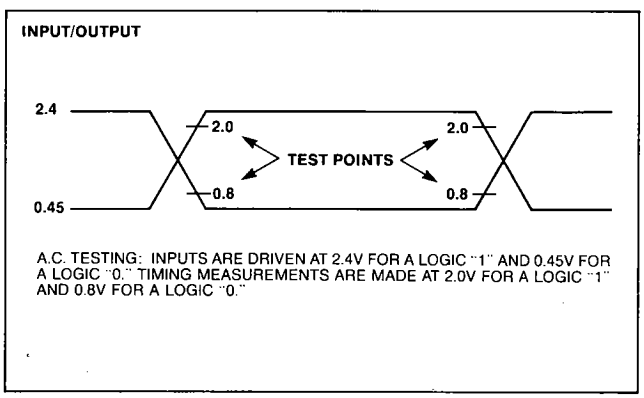
## CAPACITANCE

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $C_{IO1}$ | I/O Capacitance (GPIB Side) | | 50 | 80 | pF | $V_{IN}$ = $V_{CC}$ |
| $C_{IO2}$ | I/O Capacitance (System Side) | | 35 | 50 | pF | $V_{IN}$ = $V_{CC}$ |
| $C_{ITR}$ | Input Capacitance (T/R1, T/R2) | | 7 | 10 | pF | $V_{IN}$ = $V_{CC}$ |

## A.C. CHARACTERISTICS ($T_A$ = 0°C to 70°C, $V_{CC}$ = 5.0V ±10%, GND = 0V)

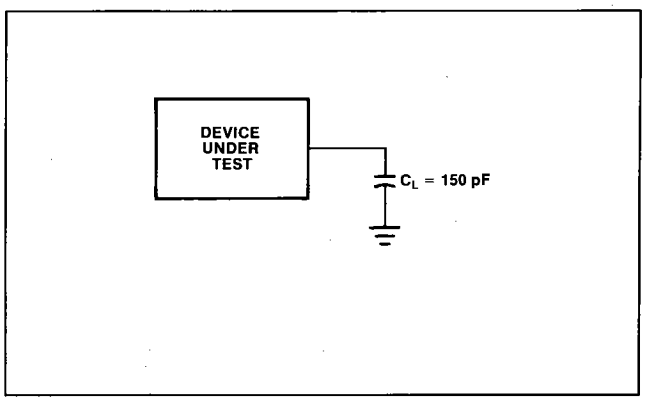
| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $t_{P1}$ | Transmitter Propagation Delay (All Lines) | 30 | ns |
| $t_{P2}$ | Receiver Propagation Delay (EOI, ATN and Handshake Lines) | 50 | ns |
| $t_{P3}$ | Receiver Propagation Delay (All Other Lines) | 60 | ns |
| $t_{PHZ1}$ | Transmitter Disable Delay (High to 3-State) | 40 | ns |
| $t_{PZH1}$ | Transmitter Enable Delay (3-state to High) | 40 | ns |
| $t_{PLZ1}$ | Transmitter Disable Delay (Low to 3-State) | 40 | ns |
| $t_{PZL1}$ | Transmitter Enable Delay (3-State to Low) | 40 | ns |
| $t_{PHZ2}$ | Receiver Disable Delay (High to 3-State) | 40 | ns |
| $t_{PZH2}$ | Receiver Enable Delay (3-State to High) | 40 | ns |
| $t_{PLZ2}$ | Receiver Disable Delay (Low to 3-State) | 40 | ns |
| $t_{PZL2}$ | Receiver Enable Delay (3-State to Low) | 40 | ns |
| $t_{MS}$ | Mode Switch Delay | 10 | μs |

### A.C. TESTING INPUT, OUTPUT WAVEFORM

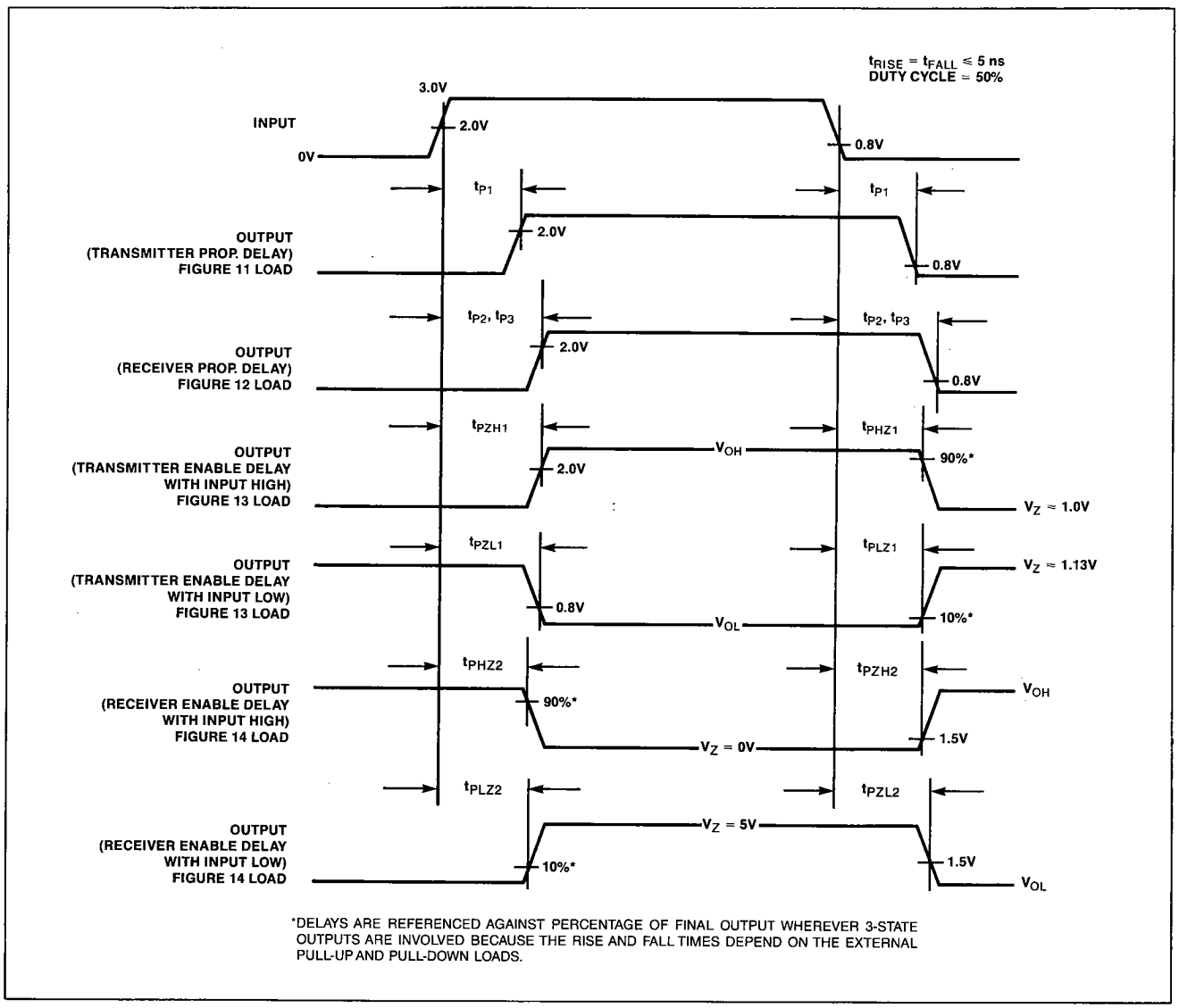



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

### A.C. TESTING LOAD CIRCUIT FOR PROPAGATION DELAYS

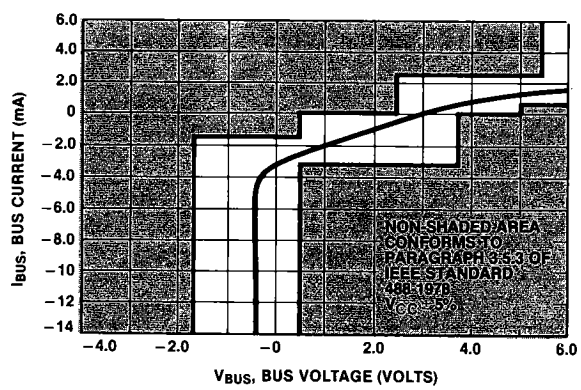


## WAVEFORMS

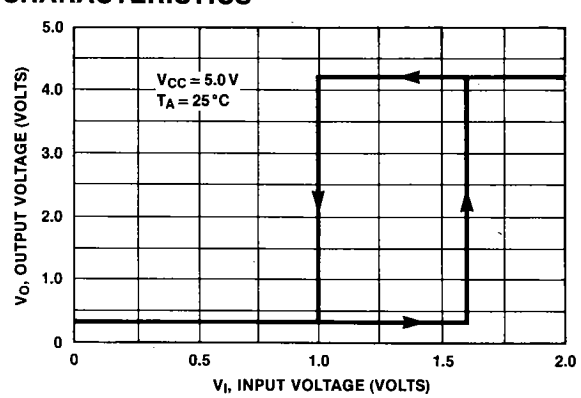



*DELAYS ARE REFERENCED AGAINST PERCENTAGE OF FINAL OUTPUT WHEREVER 3-STATE OUTPUTS ARE INVOLVED BECAUSE THE RISE AND FALL TIMES DEPEND ON THE EXTERNAL PULL-UP AND PULL-DOWN LOADS.

### BUS LOAD LINE




### TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

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